Claims

Claim 1. A system for modeling a bi-directional signal of an electric circuit, comprising:

means for maintaining a state of an input component of the bi-directional signal;

means for maintaining a state of an output component of the bi-directional signal; and

means for generating a resolved state based upon at least the input component state and output component state.

Claim 2. The system of Claim 1 wherein the resolved state is further based upon resistive data.

Claim 3. The system of Claim 1 wherein the input component state, output component state and resolved state are output to a computer file.

Claim 4. An improved pad cell model, comprising:

an input node which reflects data that is supplied to the pad cell from external sources;

an output node which reflects data that is supplied as output from the pad cell; and

a resolved node which reflects the combination of the input node and output node.

Claim 5. The pad cell model of Claim 4 wherein the resolved node also reflects the combination of resistive data.

Claim 6. The pad cell model of Claim 4 further comprising means for selectively connecting the input node to the resolved node.

Claim 7. An improved pad cell model, comprising:

an I/O pad;

an output driver;

a buffer coupled between the I/O pad and the output driver; and

an input receiver having an input and output, said input receiver comprising means for coupling the input (i) directly to the output, or (ii) to the output through a buffer.

Claim 8. A method for modeling a bi-directional signal of an electric circuit, comprising the steps of:

maintaining a state of an input component of the bi-directional signal;

maintaining a state of an output component of the bi-directional signal; and

generating a resolved state based upon at least the input component state and output component state.

Claim 9. The method of Claim 8 wherein the resolved state is further based upon resistive data.

Claim 10. The method of Claim 8 further comprising the steps of:

specifying at least one bi-directional signal of a logic design to be simulated; and

simulating the logic design.

Claim 11. The method of Claim 8 further comprising the step of selecting whether to couple the input (i) directly to the output, or (ii) to the output through a buffer.

Claim 12. A method for operating the pad cell model of Claim 4 in accordance with the method of Claim 8.